Designing with the ISL6752, ISL6753 ZVS Full-Bridge Controllers

Application Note | August 15, 2006 | AN1262.0

Introduction

The ZVS (Zero Voltage Switching) full-bridge topology has been around for many years and has become the industry's workhorse. One of the drawbacks to this topology is the additional wave shaping circuitry required to produce the correct gate drive signals. This has been resolved with Intersil products such as the ISL6752 and ISL6753. These components have not only simplified the design of the ZVS full-bridge but have included additional features that are useful to the designer.

Scope

This document provides some helpful information and tips in designing with the ISL6752 and ISL6753 for the ZVS full-bridge topology. This includes such tips as setting the resonant and synchronous rectifier timings. More helpful information is available in application notes AN1002 and AN1246.

Resonant Timing and Energy

One of the key operations for the ZVS full-bridge is setting the delays to turn on the lower MOSFETs based on the resonant timing. This is accomplished by adjusting the voltage on the RESDEL pin of the IC. As a starting point and before powering up the converter, set the voltage on RESDEL pin to 1.8V. This will set a large time delay between the upper MOSFET's transitioning and the lower MOSFET turning on. It is recommended that the synchronous rectifiers be disabled during this procedure. See "Synchronous Rectifiers" on page 3 for a method to disable the synchronous rectifiers.

With the above modifications in place, slowly bring up the supply voltage to the ZVS full-bridge and keep the load at the minimum current. Monitor the gate-source of an upper MOSFET and both the gate-source and drain-source of the lower MOSFET that is diagonally opposed. Figure 1 depicts the waveforms seen in the ZVS full-bridge:

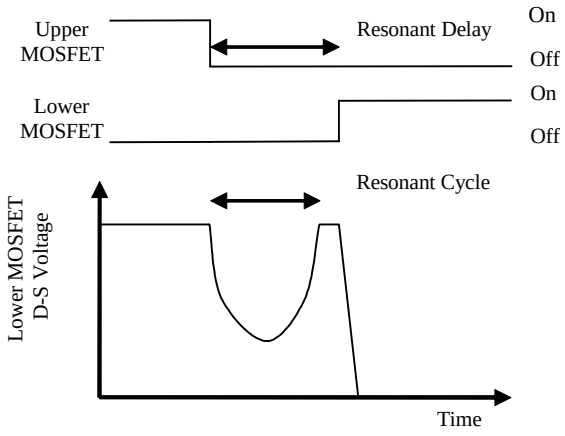

FIGURE 1. RESONANT DELAY AND TRANSITION

The waveforms should clearly show the resonant cycle on the drain-source voltage of the lower MOSFET. The turn on of the lower MOSFET was intentionally delayed beyond the resonant transition for clarity. If this resonant cycle is not seen, increase the load current slightly. The resonance is due to the inductance of the transformer and the parasitic capacitance of the drain-source node, predominantly determined by the capacitance of the MOSFETs.

The amplitude of the resonant cycle is due to the load and the amount of energy stored in the transformer inductance. Figure 2 shows the effect of varying the load on the resonant cycle:

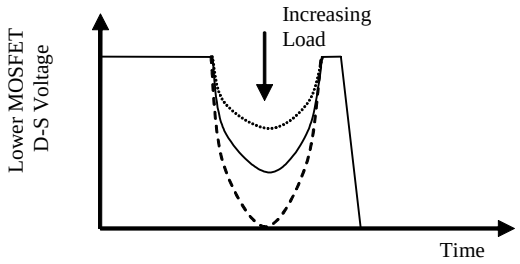

FIGURE 2. RESONANT CYCLE WITH LOAD

As the load increases, there is more energy available to charge and discharge the capacitance. There will be a point at which the drain-source voltage of the lower MOSFET reaches 0V. This is the minimum load which results in ZVS operation. When the load is further increased, the current starts to flow through the MOSFET body diode and becomes clamped to circuit ground. Figure 3 shows the effect on the resonant cycle when there is excess ZVS load current. The waveform has been expanded around the resonant cycle near 0V on the lower MOSFET drain-source voltage.

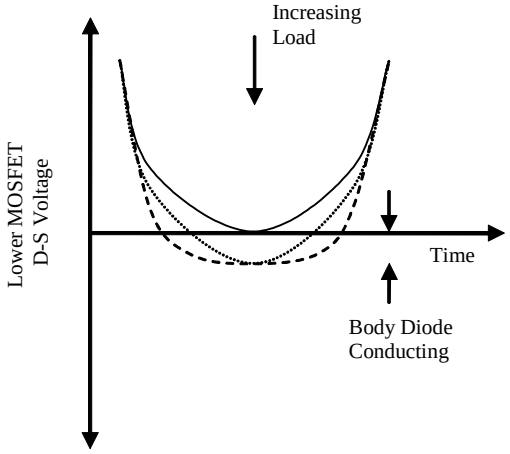

FIGURE 3. RESONANT CYCLE ABOVE MIN ZVS LOAD

During this interval the excess energy is returned to the source, but results in dissipation in the body diode. The resonant current flows through the body diode, which can exhibit reverse recovery characteristics when the resonant current reverses direction. Ideally there should be as much resonant energy as possible so that the minimum ZVS load current is as low as possible. However, once above the minimum ZVS load current, the excess resonant energy becomes disadvantageous. The extra energy is not required. The resonant current may be high enough to affect the current sense signal. This will appear as a turn on current spike, but upon closer inspection, it will be apparent that the signal is sinusoidal rather than a sharp spike. There have been circuits developed that will adjust the amount of energy stored so as not to waste energy and reduce the circulating current.

Another way of looking at this resonant cycle is to realize that this behavior is very similar to what happens in a conventional full-bridge when the MOSFETs in the bridge turn off and the leakage inductance rings with the parasitic capacitances. The difference is that the primary is clamped by the upper MOSFETs so that the ringing occurs at turn on rather than at turn off.

Resonant Delay Adjustment

The resonant delay is adjusted by changing the voltage at the RESDEL pin of the IC using a resistor divider. Decreasing the voltage will decrease the resonant delay for the timing waveforms. Ideally the resonant delay should be set to the lowest point of the resonant cycle to turn the lower MOSFET on at the minimum drain-source voltage. The resonant delay is called the resonant transition and is shown in Figure 4.

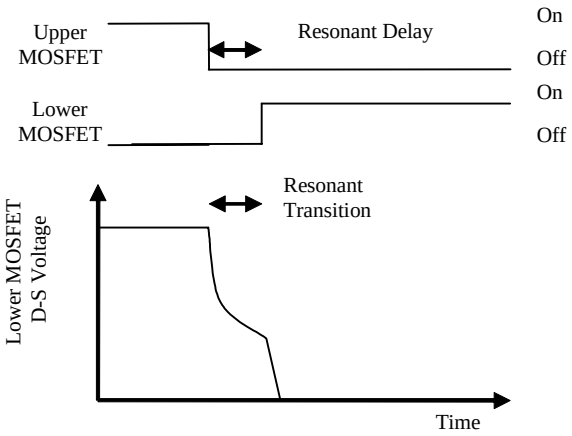

FIGURE 4. RESONANT DELAY ADJUSTMENT

Turning on at the minimum resonant voltage guarantees that the load current at which the converter will ZVS is at its minimum. However, at higher loads where there is significant amount of resonant energy, there will be some power loss due to the body diode forward voltage drop as shown in Figure 5.

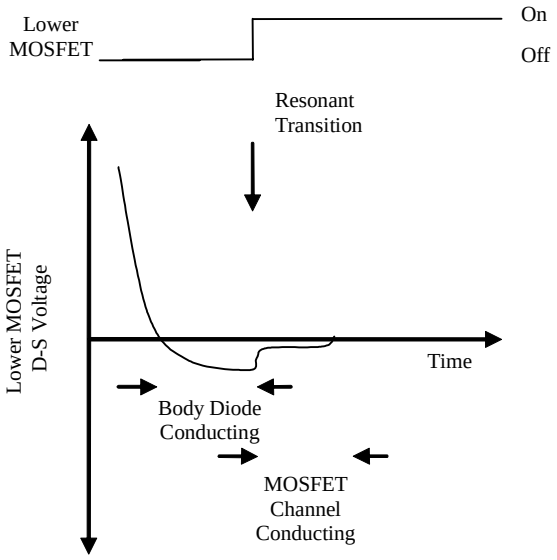

FIGURE 5. RESONANT CYCLE ABOVE MIN LOAD

The body diode is still conducting through the first half the resonant cycle until the lower MOSFET turns on, which allows the resonant current to flow through the channel of the MOSFET. As long as the I x R_{DSON} drop of the MOSFET is less than the body diode forward voltage drop, the body diode will not conduct. Even though the lower MOSFET turns on, the current does not change polarity immediately. The current's rate of change will be determined by the supply voltage divided by the leakage inductance (di/dt = V/L).

There are two possible options that can be used if the power loss or high resonant current becomes an issue. One is, turn the lower MOSFET on sooner and catch the resonant edge earlier. This reduces the time the body diode is on but will also increase the minimum load at which the converter will fully ZVS. The other is to decrease the resonant frequency by either reducing the leakage inductance or parasitic capacitance. This will reduce the time the body diode conducts and the time taken up by the resonant period for the maximum duty cycle. It's preferable to reduce the parasitic capacitance as much as possible. Reducing the leakage inductance will reduce the amount of energy stored and therefore require a higher minimum load to ZVS.

Switching Loss and EMC

In conventional full-bridges, the power loss in the MOSFETs is due to both switching and conduction loss. Typically, designers struggle to reduce the switching loss by turning the MOSFETs on/off as quickly as possible. Doing so results in higher switching noise due to the fast drain-source transition edge and creates EMC (Electro-Magnetic Compatibility) issues.

In the ZVS full-bridge this is not as clear cut. At loads above the minimum ZVS load current, the lower MOSFET's losses will be strictly due to conduction loss. However, as the load current decreases, switching loss does come into effect while conduction loss decreases. Even when the ZVS full-bridge is operating below its minimum ZVS load current, switching loss does not become a significant concern as with conventional full-bridges. The designer has flexibility in slowly turning on the lower MOSFETs. Figure 6 shows a lower MOSFET turning on when below the minimum ZVS load current:

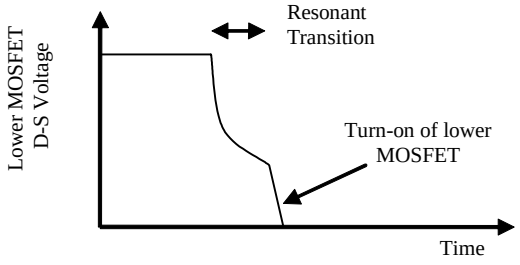

FIGURE 6. HARD SWITCHING OF LOWER MOSFET

It may be difficult to see where the resonant cycle ends and the start of the lower MOSFET turn on, if the resonant cycle is short and/or the MOSFET turns on slowly. Vary the load slowly and the two modes should be distinguishable.

A unique advantage of the ZVS full-bridge topology supported by the ISL6752 and ISL6753 ICs is that the upper MOSFETs will always zero voltage switch because the body diode is conducting before the MOSFET turns on. This is because the freewheeling currents circulate in the upper MOSFETs. However, they also carry the primary switch current and some or all of the primary freewheeling current. So the total losses for the upper MOSFETs will be higher than the lower MOSFETs when operating above the minimum ZVS load current. Normally there is a compromise between the R_{DS-ON} and the capacitance of the MOSFET, as is the case for the lower MOSFETs. For the upper MOSFETs, low R_{DS-ON} can be used to keep the conduction loss down as low as possible because there is no switching loss. Also, since this topology is typically used in high power applications, device packages such as TO-220 and TO-247 may be used. The metal tabs (connected to the drain) of the devices can be directly attached to a heatsink without any EMC issues because that node is the DC supply voltage. The lower MOSFET, however, does not share this advantage because the drain tab is switching between power supply rails. It is not uncommon to see larger devices for the upper MOSFETs compared to the lower MOSFETs. The only disadvantage is that the lower R_{DS-ON} MOSFETs have higher capacitance and will cause both the minimum ZVS load current and the resonant period to increase.

The body diodes in the upper MOSFETs conduct only until the upper MOSFETs transition. The current then flows through the MOSFET's channel.

Should reverse recovery of the body diodes become an issue, whether it's the lower or upper MOSFET, there are some options to consider. One option is to use devices optimized for body diode performance. International Rectifier's IRF840LC, for example, has a low charge body diode as compared to the standard IRF840. Another option is to reduce the R_{DS-ON} of the MOSFET, but this increases the resonant time and resonant capacitance. Infineon CoolMOS™ MOSFETs have one quarter the R_{DS-ON} of a standard MOSFET for the same die size yet the same capacitance. They reduce power loss significantly yet have very little effect on the resonance of the circuit.

Another advantage that ZVS full-bridges have in general is the clean waveforms. No snubbers are required to dampen the primary transformer voltage ringing when the MOSFETs turn off. Instead the waveforms have a sinusoidal edge equal to the resonant transition. The dV/dt rate for the drain-source voltage is less than a conventional hard-switched full-bridge. Since leakage inductance is not an issue, the primary-secondary winding spacing can be increased to reduce the primary-secondary transformer capacitance. Doing so will reduce the common mode currents through the transformer. Usually, EMC noise is significantly less with a ZVS full-bridge than a standard full-bridge.

Synchronous Rectifiers

Once the resonant delay is adjusted, the timing of the synchronous rectifiers can be investigated. The ISL6572 incorporates signals for the synchronous rectifiers with adjustable advance and delay timing with respect to the MOSFET drive signals for the bridge. This allows flexibility in adjusting the timing; however, setting up the timings on an operating unit can be frustrating. Should the synchronous rectifier turn on too soon or turn off too late, the MOSFETs will short out the secondary side of the transformer. This will result in large spikes of current in the primary which will affect the current sensing circuit. If the overlap is large enough, the converter may even experience a catastrophic failure.

To help avoid these issues, the following step-by-step instructions will aid the designer in getting the synchronous rectifiers operating without causing potential problems to the converter.

The first step is to make the following circuit modification to the synchronous rectifier circuit.

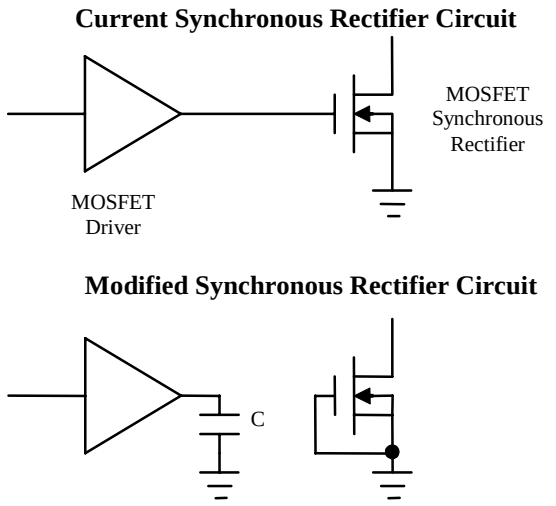

FIGURE 7. MODIFIED SYNCHRONOUS RECTIFIER CIRCUIT

Disconnect the drive signal to the MOSFET so that the MOSFET operates as a standard rectifier using only the body diode. Add a capacitor to the output of the driver to mimic the gate load of the synchronous rectifiers. The value of the capacitor should equal the total gate charge divided by the maximum gate drive voltage. The total gate charge can be found in the manufacturer's datasheet of the MOSFET device. Short the gate-source of the MOSFET to ground so it remains off and the current is conducted through the body diode. Fast rising drain voltages can turn the MOSFET on through the Miller capacitance. Shorting the gate-source to ground will prevent this from occurring. Repeat the procedure for all synchronous rectifiers on the secondary output. The output will behave like a standard rectifier output with diodes that have high reverse recovery charge. R-C snubbers across the body diodes may be required to dampen any excessive voltage ringing.

Once the procedure is completed, power up the converter with a light load and investigate the MOSFET Output Driver waveform and the MOSFET D-S Voltage. The basic concept in driving MOSFETs in synchronous rectifier applications is to turn on the MOSFET after the body diode conducts and turn off the MOSFET before the current starts to reverse direction in the MOSFET. With this procedure, any issue with the drive signal can easily be identified and corrected before reconnecting the synchronous rectifiers. The required waveforms are shown in Figure 8.

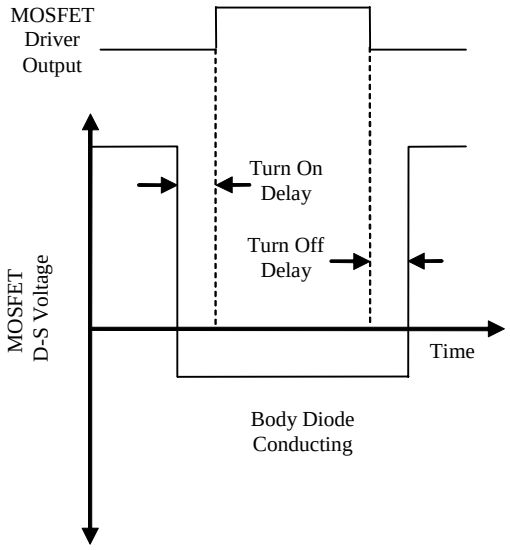

FIGURE 8. TIMING WAVEFORMS SETUP

As a starting point, the Turn On Delay and Turn Off Delay should be set at around 100ns at full load. The timing on the ISL6752 allows advance or delay between the bridge MOSFETs and synchronous rectifiers. This is a phase relation adjustment where both the turn on and turn off edges will move in unison. Most likely the design will require one edge to be delayed through an R-C-D network so that it can be fine tuned. One such circuit is shown in Figure 9.

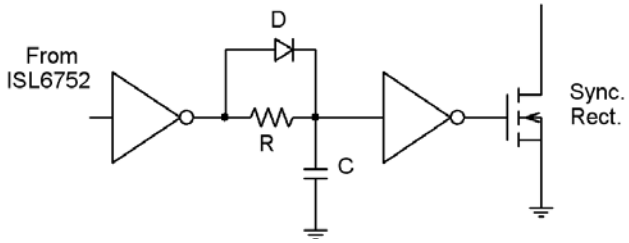

FIGURE 9. R-C-D NETWORK

This circuit receives the synchronous rectifier signals OUTLLN or OUTLRN from ISL6752. The timing is adjusted through VADJ so that the turn on delay is correct. Then the R-C network is adjusted so that the turn off delay is reasonable. Once this is done, the capacitor and gate-source short can be removed and the MOSFETs can be reconnected to the driver. This method of initially powering up the synchronous rectifiers prevents unnecessary debug time. Once the ZVS full-bridge is powered up, the waveforms in Figure 10 on the synchronous rectifiers may be observed.

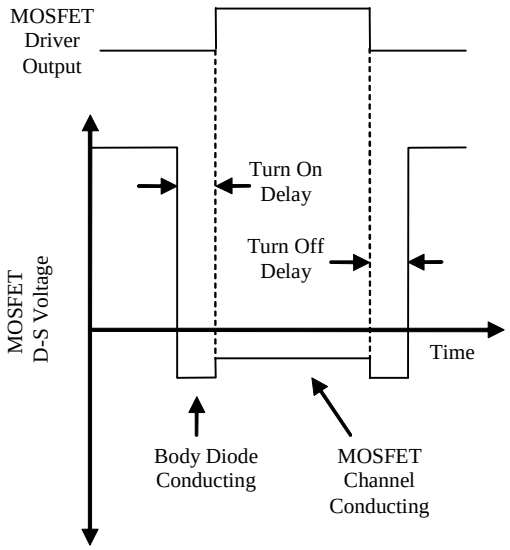

FIGURE 10. TIMING WAVEFORMS FOR SYNCHRONOUS RECTIFIER

This shows that the body diode is conducting before and after the MOSFET is turned on and the current is flowing through the MOSFET channel when the MOSFET is on.

The efficiency of the converter due to the synchronous rectifiers is directly related to the time the body diodes are conducting. Reducing this time can significantly improve the efficiency. However, reducing this time is not without risk. The timings should be checked while varying the line and load conditions. For example, when the load is varied, rise and fall rates of the current (di/dt) remain the same because the voltage developed across the leakage inductance and traces are independent of the load. Therefore, it will take more time to transition the current at full load than at light loads. The timings need to be adjusted for the worst case condition. Since temperature affects the switching characteristics of the synchronous rectifiers, the timings must be verified over the operating temperature range as well.

If there is too much variability, different driving schemes should be considered. One such method, is not turning on the MOSFET until the transformer voltage has risen on the other MOSFET. A self driven scheme for turn on may be used, but use the technique described in this document for turn off. Another option is to use saturable cores in the series with the drains of the MOSFETs or on the secondary windings. Saturable cores such as Toshiba's SPIKE KILLERS® cores are suitable. This will block the current for a period of time should the synchronous rectifiers overlap and cause cross conduction (shoot-through).

Temperature will have an effect on the timings. There are two paths from the ISL6752 to drive the MOSFETs. One for the primary side MOSFETs and the other is through the synchronous rectifiers. Both paths will have different propagation delays and will vary differently with temperature. There will even be some variation with the ISL6752. A work around to this problem is to replace one of the resistors with a thermistor for the voltage divider on VADJ for the ISL6752. This would vary the delays based on temperature. However, if an R-C-D network is used as shown in Figure 9, the resistor for the R-C-D must also be replaced with the thermistor to counter the change in turn on delay with temperature.

There may also an issue with the variability in component values used to set the timing. The solution is to use components with tighter tolerances.

With all the issues identified, the minimum turn on and turn off delay should not be less than 50ns for a conservative design. It is tempting to reduce these delays because of significant improvement in efficiency, but there is a risk of overlap and cross conduction.

Rectifier Output

Not all designs require synchronous rectification and the ISL6753 was developed for this reason in mind. Synchronous rectification with today's low R_{DS-ON} MOSFETs is practical up to about 15V output. For output voltages above that, the performance improvements do not justify the cost and complexity. As MOSFET technology advances, the voltage limitation will improve.

Conventional rectifier outputs offer their own set of challenges. The rectifier of choice in designing the output stage is the Schottky diode. These diodes have a typical forward drop of 0.3V as opposed to 0.7V for standard PN junctions. This is significant in power loss at high output current.

However, today's Schottky diodes are limited to 200V for reverse breakdown voltage. Further, at high currents it is not recommended to use Schottky diodes with 150V or higher ratings. Schottky diodes have a guard ring structure that is essentially a PN junction in parallel with the Schottky barrier. Under normal operating conditions, the PN junction is not active. However, with high voltage breakdown devices, the device doping is low, resulting in an increase in the forward voltage required to turn the Schottky diode on. Additionally, the light doping causes the bulk resistance to be higher, and at high currents, the IR drop becomes significant. This can result in the PN junction becoming forward biased at high currents and the diode will have reverse recovery charge behavior.

If PN diodes are the only option, then diodes with the lowest reverse recovery charge and lowest voltage rating are recommended. The amount of stored charge in a given family of PN diodes will be proportional to the reverse voltage rating.

Regardless of the rectifier selection, the devices will require voltage snubbing networks. One method uses an R-C

network across the diode. The voltage on the diode rings because the capacitance of the diode resonates with the transformer leakage and other parasitic inductances when the voltage across the junction reverses. Placing a series R-C network across the diode changes the characteristics of the resonant circuit as shown in Figure 11.

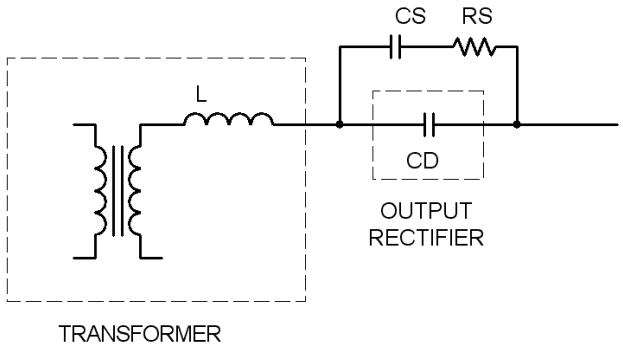

FIGURE 11. R-C SNUBBER

The idea of the R-C snubber is to make CS, 2 to 10 times larger than the average capacitance of the diode, CD. This effectively “swamps” out the effects of CD in the circuit. RS is set to 2 to 5 times $\sqrt{L/(CD+CS)}$ which will provide damping to the diode voltage. L can be determined by the resonant frequency with CD and CS. This procedure will provide a good starting point. There are some pitfalls that need to be avoided.

- If CS is too small, the R-C snubber will have no effect.
- If CS is too large, there will be a large spike of current to charge and discharge CS. This will show up as an initial current spike in the current switch waveform. This will cause the converter to behave abnormally. If CS is changed, then RS needs to be adjusted.
- If RS is too small, there will not be enough damping. Resonant frequency will depend on CD+CS.
- If RS is too large, the R-C snubber will have no effect. Resonant frequency will depend on CD only.
- The power dissipated in the snubbers are directly proportional to the switching frequency and the value of CS.
- If PN diodes are used there will be reverse recovery charge as an added effect. The snubber will require more dampening.

Another method for snubbing output rectifiers is the use of saturable cores. This is discussed in more detail in application note AN1246.

Another major issue with conventional rectifier outputs is that at low output current, the inductor current becomes discontinuous. This occurs when the output current falls below one half of the inductor ripple current. In this mode, the converter has 3 modes of operation: Ton, charging the output inductor, Toff, discharging the output inductor and Trelax where the output inductor current is zero. This is shown graphically in Figure 12.

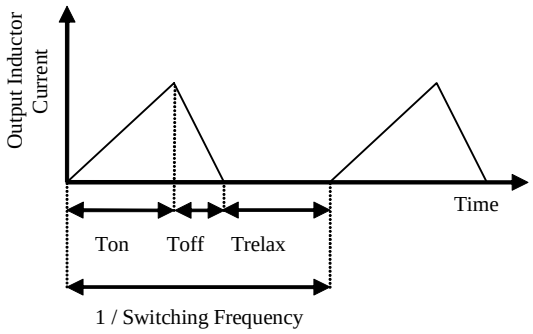

FIGURE 12. DISCONTINOUS CONDUCTION MODE

In this mode of operation, V_{OUT} is no longer the simple relationship indicated in Equation 1 for continuous conduction mode (CCM).

$$Vout = Ton \times Fsw \times Vin \quad \text{(EQ. 1)}$$

Instead, it is a complex relationship based on energy. The on time, Ton, is a function of the load current, output inductance, input voltage, output voltage, and switching frequency. Since the transfer function of the converter has changed, some unique problems occur.

The converter design is usually compensated for stability with the assumption of CCM operation. If the converter goes discontinuous, there is a chance the converter will become unstable because the transfer function has changed. Careful control loop compensation design will prevent this.

In discontinuous conduction mode (DCM), as the output current decreases, Ton will also decrease. There will be a point where the required Ton will be less than the minimum on time the PWM controller is capable of. At this point, pulse skipping occurs. Since the minimum output pulses exceed the required duration, the output is maintained by omitting pulses so that the long term average duty cycle is correct. The output maintains regulation, but output ripple performance degrades.

There are ways to lessen these issues by keeping the converter operating in CCM at lower output currents. One way to prevent DCM operation is to use a bleed resistor on the output so that when the converter is at minimum load, the bleed resistor draws enough current to maintain CCM operation. To improve efficiency, this bleed resistor can be activated only under light loads. This is an effective, if inelegant, method.

A better method is to use inductor core materials such as Molypermalloy (MPP)®, or use a step gapped inductor so that the inductor is non-linear with load. The desired behavior is to have the inductance increase as load current decreases. Inductors designed with MPP® core material can

have 3X the 0A inductance when compared to normal operating current. This can reduce the minimum load at which the inductor becomes discontinuous by a factor of 3. The stepped gap inductor design varies the gap distance across the face of the center leg. This effectively tailors the inductance as a function of current. Like the MPP® designs, the inductor will have higher inductance at lighter loads. Inductors with this behavior are often referred to as swinging chokes.

Efficiency

The ZVS full-bridge topology does offer an improvement in switching losses. However, it only affects the primary side MOSFETs. For high input voltage designs, this is significant. Additionally, no primary side snubbers are required. The leakage inductance of the transformer is clamped so that no power is wasted in dampening the ringing or dissipating the excess energy.

However there are drawbacks and some are listed below:

- The primary current needs to carry the freewheeling current and the switch current. The primary transformer winding must be sized to handle the additional RMS current.
- One of the upper MOSFETs is always conducting the freewheeling current through the body diode. For high voltage designs this is usually not an issue because the forward voltage drop of the body diode is comparable to the I x R_{DSON} voltage drop of an upper MOSFET in a typical design. For low input voltage designs this becomes an issue because the body diode forward voltage drop is significant when compared to the supply voltage and the primary currents are high.
- The resonant time reduces the allowed maximum duty-cycle. Because of this, the primary-secondary transformer turns ratio must be reduced to maintain output voltage regulation for the input voltage range. If the turns ratio is reduced, the primary side current will increase at a given load.

All these behaviors can impact the efficiency negatively.

Even though there is no switching loss in the bridge MOSFETs, there is a practical limitation to the frequency of operation. As the frequency increases, the resonant time becomes a more significant portion of the maximum duty-cycle. To compensate, the primary to secondary turns ratio has to decrease and therefore, the primary current will increase. The savings in ZVS will be eroded by the increase in conduction loss in the primary side MOSFETs. A possible technique to reduce the resonant time is to bypass the body diode with a Schottky diode in series with the drain of the MOSFET and use a low capacitance ultra-fast diode as the new body diode. This can reduce the resonant time by a factor of 10 and practical 1MHz ZVS full-bridge have been developed.

However, operating magnetic components at high frequency poses problems as well. Normally, as the operating frequency increases, the size of the magnetic components decreases. However there will be a point where eddy currents [1] and core losses become an issue and the transformer size will need to increase to compensate. If saturable cores are used to help steer the secondary currents, the frequency limitation starts at about 150kHz to 200kHz.

If synchronous rectifiers are used, the performance improvements decline as the frequency increases. There is a fixed minimum turn on and turn off time as well as a minimum body diode conduction time. As the frequency increases, the amount of time the body diode is conducting remains constant but the time the MOSFET channel conduction is on within a switching cycle will decrease. The result is the duty cycle for MOSFET channel conduction decreases as frequency increases and the synchronous rectifier becomes less efficient [2, 3].

With all these issues, the practical limitation for the operating frequency is 150kHz to 400kHz for the ZVS full-bridge.

Comparison of Different ZVS Full-Bridge Algorithms

This document discussed one type of ZVS full-bridge in which current freewheels in the upper MOSFETs. There is another type of ZVS full-bridge that is more commonly known as “Phase-Shifted ZVS Full-Bridge”. In this topology, the freewheeling current circulates in either the MOSFETs in the upper or lower sections of the bridge. In the Phase-shifted algorithm, the drive signals to the MOSFETs are always 50% duty cycle, but the phase difference between the left side and right side of the bridge determines the duty-cycle applied to the main transformer. For more detail information on a ZVS phase-shift design see application note, AN9506.

The following lists out some of the advantages of the Phase-Shifted ZVS Full-Bridge:

- The freewheeling current will always flow through the MOSFET channel as opposed to one of the body diodes for the ZVS full-bridge discussed here. Assuming the voltage drop due to the R_{DS-ON} is lower than the forward voltage drop of the body diode. This is advantageous with low input voltage designs.
- Since the gate drive signals are always at 50%, the gate drive transformer becomes easier to design. With PWM gate drive signals there is always an issue of voltage ringing on the transformer, which may turn the MOSFET back on at the wrong time.

Advantages of the ZVS Full-Bridge:

- The control logic required to generate the MOSFET signals for Phase-Shifted ZVS Full-Bridge is more complex because the modulation is phase related.
- The ZVS full-bridge discussed here freewheels in the upper MOSFETs. Since the upper MOSFETs carry both the switch and freewheeling current, they will dissipate more power than the lower MOSFETs. Since this extra power is in the upper MOSFETs, those devices can be cooled more easily since they can be tied directly to a heatsink without generating EMI.

From these two ZVS type full-bridges, there have been circuit modifications that have been added to overcome some of the drawbacks. A small sample of these modifications is listed below:

- Adding an inductor in series with the primary winding of the transformer to effectively increase the leakage inductance. This improves the minimum load at which the converter can achieve ZVS operation.
- Adding a saturable inductor in series with the primary winding of the transformer to effectively increase the leakage inductance during zero voltage transitions.
- Add both an inductor and a capacitor in series with the primary winding of the transformer. Set the resonance to the switching frequency to form a resonant converter that will ZVS and ZCS (zero current switch).

Layout Guidelines

Like any other switching power regulator, ISL6752, ISL6753 and the associated circuitry require that good layout guidelines be followed. One of the most common mistakes made is using a ground plane and assuming that all the noise issues due to layouts can be resolved. Sometimes the opposite is true. Not only could the noise be worse but there is added capacitance to the ZVS full-bridge which hurts its minimum ZVS load current and increases the PWB cost because of extra internal layers.

Figure 13 shows an example circuit with the ground wired as one large plane.

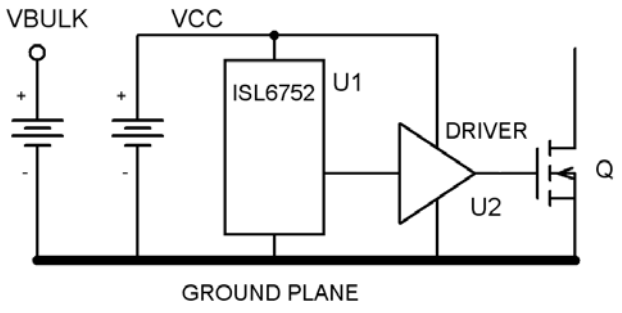

FIGURE 13. LAYOUT WITH GROUND PLANE

VBULK supplies power to the ZVS full-bridge stage and Q is one of the lower MOSFETs. VCC supplies power to U1, which in this example is the ISL6752 PWM, and to U2, a generic MOSFET driver. In reality, the ground plane still has some resistances and inductances. Keep in mind, that there will be pulses of current flowing and that the resistance of the ground plane will be due to skin effect. Figure 14 shows the equivalent circuit with current flowing from the ZVS Full-bridge.

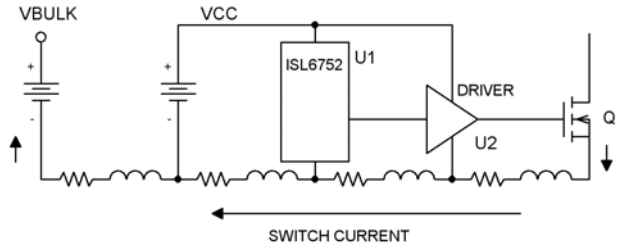

FIGURE 14. EQUIVALENT R AND L

Every time Q turns on, there is a pulse of current that will flow from the MOSFET through the ground plane and back to the bulk supply generating voltage spikes which will affect the analog circuitry on U1. Even if the VBULK supply were moved next to the MOSFET (Q) there will be some effect throughout the ground plane. When Q switches, the ground plane is effectively a matrix of R's and L's. From another perspective, the pulse currents generated by the switching action of the MOSFET (Q) is like throwing a rock in a pond. The ripples it generates are the electrical noise. Even though the noise sensitive circuits are far away, the ripples will still reach them.

Granted, a ground plane will be superior to using a single wire in a poor layout because the effective impedance will be lower, but it is not good design practice. This is the reason why going to a ground plane seems to help the noise issues, but a properly connected layout will be even better.

The preferred way is to connect the circuit so that U1's ground does not share the high current ground as shown in Figure 15.

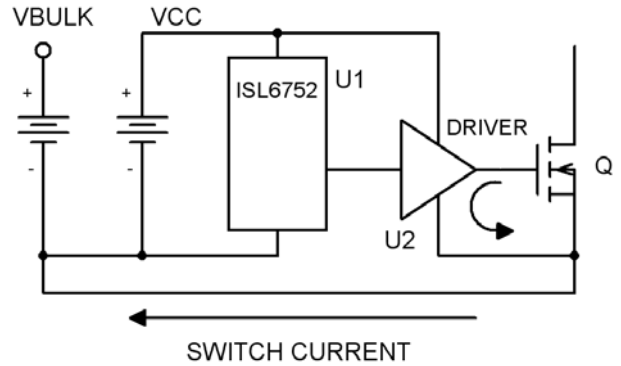

FIGURE 15. SEPARATING HIGH CURRENT PATHS

Instead of allowing the switch current to go through the ground plane, wire a path directly between the source of the MOSFET (Q) to the bulk supply, VBULK. This allows the Instead of allowing the switch current to go through the

ground plane, wire a path directly between the source of the MOSFET (Q) to the bulk supply, VBULK. This allows the switch current to directly flow from the MOSFET (Q) to the bulk supply and not affect U1.

The ground of the driver must be tied directly to the source of MOSFET (Q) because there is a spike of current when the driver discharges the MOSFET capacitance. There will also be a spike of current going into the positive supply of the driver when charging the MOSFET capacitance. This should not affect the rest of the circuit because the decoupling capacitor of the driver (between the positive supply pin and return of the driver) will circulate the current around the driver and its decoupling capacitor. Therefore, the positive supply of the driver does not have to be connected directly to VCC to bypass U1. The connection between the returns for VBULK and VCC maintains a DC reference connection. Theoretically, no current will flow.

At first glance, there may be an issue with noise between the returns of U1 and U2. This is true because the switch current flowing between the MOSFET and the bulk supply will generate some voltage spikes. This will also be true when U2 discharges the MOSFET gate capacitance. However, the signal between U1 and U2 is not analog but digital. You can have significant noise levels and not affect the behavior of U1 and U2.

Special care should be taken for connecting the analog circuitry for U1. The PWM IC such as U1 contains the reference voltage used for regulation. All the analog components must be then referenced to U1's ground to eliminate a ground shift. One method is to use a star grounding pattern as shown in Figure 16.

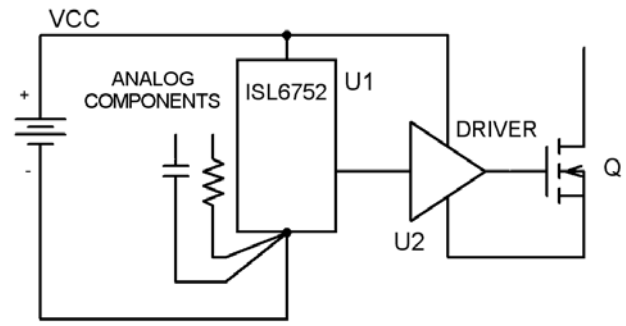

FIGURE 16. WIRING U1

However, it's not always easy to wire a star pattern when there is significant number of components. In this case, it's acceptable to set up a ground plane under U1 and extended it out to cover some of the analog circuitry. The ground plane should be tied directly to the ground of U1 and then a wire from the ground of U1 back to the VCC ground. This ground plane is considered a "quiet ground" since there are no switch currents flowing in this plane. The quiet ground plane also adds a small amount of capacitance between it and the pins of U1. This helps reduce noise on some of the critical pins of U1.

A final issue to be concerned with on the layout is the drive paths for the primary side MOSFETs and synchronous rectifiers. The circuitry driving the MOSFETs from the ISL6752 must be symmetrical so as not too cause unmatched propagation delay. The timings for resonant periods or turn on and turn off delays could be less than 50ns.

Conclusion

This document has some helpful tips in designing with the ISL6572, ISL6573 and the ZVS Full-bridge converter. For further helpful information, see application notes AN1002 and AN1246.

References

[1] Lloyd H Dixon Jr., "Eddy Current Losses in Transformer Windings and Circuit Wiring", SEM600 Unitrode Seminar, 1988

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